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PATENT APPLICATION TRANSMITTAL LETTER

Transmitted herewith for filing is the patent application of:

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2. Title: Semiconductor Device And Method Of Manufacturing The Semiconductor Device

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Enclosed are:

X	10	Sheets of Drawings
	X	Formal
	_____	Informal
X		Assignment of invention to Semiconductor Energy Laboratory Co., Ltd.
X	29	Pages of Specification
X	10	Pages of Claims
X		Abstract of The Disclosure
_____		Statement of Small Entity
X		Declaration and Power of Attorney

__X__ Information Disclosure Statement

__X__ Appointment of Associate Attorneys

Applicant claims priority under 35 USC §119 to the following foreign application:

Serial no. 11-228944 filed August 12, 1999 in Japan.

__X__ A certified copy of this priority document is enclosed herewith.

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Claims as Filed

	Number Filed		Number Extra	Rate	Fee
Total	24	-20	4	(small entity) x 9 (others) x 18	$72.00
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SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device having a circuit structured by an inverse-stagger type or bottom gate type thin film transistor (hereinafter referred to as "TFT") using a semiconductor film, and a method of manufacturing the semiconductor device. In particular, the present invention relates to a technique which is preferably applicable to an electro-optical device represented by a liquid crystal display device and an electronic device on which the electro-optical device is mounted. In the present invention, the semiconductor device is directed to all of devices that function using the semiconductor characteristics, and the electro-optical device and the electronic device on which the electro-optical device is mounted fall under the category of the semiconductor device.

2. Description of the Related Art

At present, in a note type personal computer (note personal computer) and a portable information terminal, a liquid crystal display device is employed for displaying an image or character information. Since an active matrix liquid crystal display device can obtain a high-fine image as compared with a passive liquid crystal display device, the active matrix liquid crystal display device is preferably employed for the above purpose. The active matrix liquid crystal display device is structured in such a manner that TFTs which function as active elements are arranged in a matrix in correspondence with the respective pixels in a pixel

section. Each of those TFTs are normally formed of an n-channel TFT and controls a voltage which is applied to liquid crystal for each of the pixels as a switching element to conduct a desired image display.

There is the inverse-stagger type (or bottom gate type) TFT in which the active layer is formed of an amorphous semiconductor film. The amorphous semiconductor material is preferably formed of an amorphous silicon film. Since the amorphous silicon film can be formed on a large-area substrate at a low temperature of 300 °C or less, it is considered to be a material suitable for mass production. However, the TFT the active layer of which is formed of the amorphous silicon film is small in the field effect mobility to the degree of about 1 cm^2/Vsec. Under the above circumstances, the drive circuit for conducting the image display is formed in an LSI chip and mounted by a TAB (tape automated bonding) system or a COG (chip on glass) system.

The active matrix liquid crystal display device thus structured is widely applicable to not only a note personal computer but also a 20-inch grade TV system, and demands for high precision and high aperture ratio have been increasingly raised in order to improve the image quality while a screen size has been large in area. For example, a document of "The Development of Super-High Aperture Ratio with Low Electrically Resistive Material for High-Resolution TFT-LCDs", S. Nakabu, et al., 1999 SID International Symposium Digest of Technical Papers, pp. 732-735 has reported a technique of manufacturing a liquid crystal display device which is UXGA (1600 x 1200) in pixel density and 20 inches in size.

In order to supply and spread the above-mentioned products on market, there are required to improve the productivity and lower the costs while enhancing the reliability. In the active matrix liquid crystal display device, the TFTs are formed on a substrate by using a

plurality of photomasks through the photolithography technique. In order to improve the productivity and also improve the yield, a reduction in the number of processes is considered as effective means. Specifically, it is necessary to reduce the number of photomasks required for manufacturing the TFTs. The photomask is used to form a photo-resist pattern on the substrate with a mask during an etching process in the technique of the photolithography. Therefore, if one photomask is used, there added processes for resist coating, pre-baking, exposing, developing, post-baking, etc., processes for forming a film, etching, etc., which are conducted before and after the former processes and processes for separating the resist, cleaning and drying, etc., resulting in a complicated work.

SUMMARY OF THE INVENTION

The present invention has been made in order to solve the above problems, and therefore an object of the present invention is to realize a reduction of the manufacturing costs and an improvement of the yield by reducing the number of processes for manufacturing the TFTs in an electro-optical device and a semiconductor device which are represented by an active matrix liquid crystal display device.

In order to achieve the above object, according to one aspect of the present invention, there is provided a semiconductor device, comprising:

a first interlayer insulating layer made of an inorganic material and formed on an inverse stagger type (or bottom gate type) TFT with a channel formation region which is formed of a semiconductor layer having an amorphous structure on a substrate;

a second interlayer insulating layer made of an organic material and formed on the first interlayer insulating film;

a pixel electrode formed in contact with the second interlayer insulating layer; and

an input terminal portion formed along an end portion of the substrate and electrically connected to a wiring of another substrate;

wherein the input terminal portion includes a first layer made of the same material as that of a gate electrode and a second layer made of the same material as that of the pixel electrode. With the above structure, the number of photomasks used in the photolithography technique is reduced to 5.

According to another aspect of the present invention, there is provided a semiconductor device, comprising:

a first interlayer insulating film made of an inorganic material and formed on an inverse stagger type (or bottom gate type) TFT with a channel formation region which is formed of a semiconductor layer having an amorphous structure on a substrate;

a pixel electrode formed in contact with the first interlayer insulating film formed on a gate electrode of the TFT; and

an input terminal portion formed along an end portion of the substrate and electrically connected to a wiring of another substrate;

wherein the input terminal portion includes a first layer made of the same material as that of a gate electrode and a second layer made of the same material as that of the pixel electrode.

According to still another aspect of the present invention, there is provided a method of manufacturing a semiconductor device, comprising:

a first step of forming a gate electrode and a first layer of an input terminal portion which is electrically connected to a wiring on another substrate on a substrate having an insulating surface;

a second step of forming a gate insulating layer on the gate electrode;

a third step of forming a semiconductor layer having an amorphous structure on the gate insulating layer;

a fourth step of forming a semiconductor layer containing one-conductive type impurities therein on the semiconductor layer having the amorphous structure;

a fifth step of forming a source wiring and a drain wiring in contact with the semiconductor layer containing the one-conductive type impurities;

a sixth step of removing parts of the semiconductor layer containing the one-conductive type impurities and the semiconductor layer having the amorphous structure with the source wiring and the drain wiring as masks;

a seventh step of forming a first interlayer insulating layer made of an inorganic material on the source wiring and the drain wiring;

an eighth step of forming a second interlayer insulating layer made of an organic material on the first interlayer insulating layer;

a ninth step of selectively removing the first interlayer insulating layer, the second interlayer insulating layer and the gate insulating layer to expose the first layer of the input terminal portion; and

a tenth step forming an pixel electrode and a second layer of the input terminal portion on the second interlayer insulating film.

According to yet still another aspect of the present invention, there is provided a method of manufacturing a semiconductor device, comprising:

a first step of forming a gate electrode and a first layer of an input terminal portion which is electrically connected to a wiring on another substrate on a substrate having an insulating surface;

a second step of forming a gate insulating layer on the gate electrode;

a third step of forming a semiconductor layer having an amorphous structure on the gate insulating layer;

a fourth step of forming a semiconductor layer containing one-conductive type impurities therein on the semiconductor layer having the amorphous structure;

a fifth step of selectively removing the gate insulating layer to expose the first layer of the input terminal portion;

a sixth step of forming a pixel electrode and a second layer of the input terminal portion in contact with the gate insulating layer;

a seventh step of forming a source wiring and a drain wiring in contact with the semiconductor layer containing the one-conductive type impurities;

an eighth step of removing parts of the semiconductor layer containing the one-conductive type impurities and the semiconductor layer having the amorphous structure with the source wiring and the drain wiring as masks; and

a ninth step of forming a first interlayer insulating layer made of an inorganic material on the source wiring and the drain wiring.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features and advantages of this invention will become more fully apparent from the following detailed description taken with the accompanying drawings in which:

Figs. 1A and 1B are top views and cross-sectional views showing processes of manufacturing a pixel TFT and an input terminal portion;

Figs. 2A and 2B are top views and cross-sectional views showing processes of manufacturing the pixel TFT and the input terminal portion;

Figs. 3A and 3B are top views and cross-sectional views showing processes of manufacturing the pixel TFT and the input terminal portion;

Figs. 4A and 4B are top views and cross-sectional views showing processes of manufacturing the pixel TFT and the input terminal portion;

Fig. 5 is a top view and a cross-sectional view showing a process of manufacturing the pixel TFT and the input terminal portion;

Fig. 6 is a cross-sectional view showing the structure of a liquid crystal display device;

Fig. 7 is a cross-sectional view showing the structure in which the liquid crystal display device is mounted;

Figs. 8A and 8B are cross-sectional views for explanation of the structure of a gate electrode;

Fig. 9 is a diagram for explanation of a taper structure on an end portion of the gate electrode;

Fig. 10 is a top view for explanation of an arrangement of a pixel portion and an input terminal portion of the liquid crystal display device;

Figs. 11A and 11B are cross-sectional views for explanation of the structure of the input terminal portion; and

Figs. 12A to 12F are diagrams showing examples of the semiconductor device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Now, a description will be given in more detail of preferred embodiments of the present invention with reference to the accompanying drawings.

(First Embodiment)

A first embodiment of the present invention will be described with reference to Figs. 1A, 1B, 2A and 2B. This embodiment shows a method of manufacturing a liquid crystal display device, and a method of forming an inverse stagger type TFT of a pixel portion on a substrate and fabricating a storage capacitor connected to the TFT will be described in detail in the order of processes. Also, those figures show a process of fabricating an input terminal portion disposed on an end portion of the substrate for electric connection to a wiring of a circuit disposed on another substrate. In Figs. 1A, 1B, 2A and 2B, portions (I) show top views whereas portions (II) show cross-sectional views taken along a line A-A'.

Referring to Fig. 1A, a substrate 101 may be made of a glass substrate such as barium boro-silicate glass or alumino boro-silicate glass which is represented by #7059 glass or #1737 glass made by Corning Inc. Alternatively, a stainless substrate or a ceramic substrate on which an oxide silicon film a nitride silicon film or the like is formed, etc., may be employed as the substrate 101.

A gate electrode 102, a gate wiring 102', a storage capacitor wiring 103 and a terminal 104 of an input terminal portion may be desirably made of a low-resistive electrically

conductive material such as aluminum (Al). However, since a single substance of Al suffers from such problems that it is low in heat resistance and is liable to be corroded, the above members are made of Al combined with a heat-resistant electrically conductive material. The heat-resistant electrically conductive material may be made of an element selected from titanium (Ti), tantalum (Ta) or tungsten (W), an alloy that contains any one of the above elements, an alloy film that combines the above elements together, or a nitride that contains any one of the above elements. In addition, the above members may be made of the combination of only the above heat-resistant electrically conductive materials.

The selection of the above materials is appropriately determined in accordance with the screen size of the liquid crystal display device. The heat resistant electrically conductive material which is about 10 Ω in area resistance and about 5 inches or less in screen size is adaptable to the liquid crystal display device. However, the heat resistant electrically conductive material is not always adaptive to the liquid crystal display device of the screen size more than 5 inches. This is because if the drawing-around length of the gate wiring connected to the gate electrode on the substrate becomes necessarily large, a problem of a wiring delay cannot be ignored. For example, in the case where the pixel density is VGA, 480 gate wirings and 640 source wirings are formed, and in the case where the pixel density is XGA, 768 gate wirings and 1024 source wirings are formed. The resistance of the gate wirings are determined in accordance with the thickness and the width of the wiring in addition to the specific resistance of the material to be used, but naturally limited by the combination with the aperture ratio, and since the pixel density becomes higher, fining is required. In the case where the screen size of the display region is 13 inch class, the length of the diagonal line is 340 mm, and in the case where the screen size is 18 inch class, the length is 460 mm. In this case, in order

to realize the liquid crystal display device, it is naturally desirable that the gate wiring is made of a low-resistive electrically conductive material such as Al.

Therefore, the gate electrode and the gate wiring are made of the combination of the heat-resistant electrically conductive material with the low-resistive electrically conductive material. The proper combination of the materials will be described with reference to Figs. 8A and 8B. If the screen size is 5 inches or less, as shown in Fig. 8A, there is applied a structure of laminating an electically conductive layer (A) 801 made of nitride of the heat resistant electrically conductive material and an electically conductive layer (B) 802 made of the heat resistant electrically conductive material. The electrically conductive layer (B) 802 may be made of an element selected from Al, Ta, Ti or W, an alloy that contains any one of the above elements, or an alloy film that combines the above elements together. The electrically conductive layer (A) 801 is formed of a tantalum nitride (TaN) film, a tungsten nitride (WN) film, a titanium nitride (TiN) film or the like. Also, as shown in Fig. 8B, an electically conductive layer (A) 803 made of nitride of a heat-resistant electrically conductive material, an electically conductive layer (B) 804 made of a low-resistive electrically conductive material and an electically conductive layer (C) 805 made of nitride of a heat-resistant electrically conductive material are laminated one on another so as to be adaptive to the large screen. The electrically conductive layer (B) 804 made of the low-resistive electrically conductive material is made of a material containing aluminum (Al) and uses 0.01 to 5 atomic% of Al containing scandium (Sc), Ti, silicon (Si) or the like in addition to pure Al. The electrically conductive layer (C) 805 has the effect of preventing hillock from occurring in Al of the electrically conductive layer (B) 804.

In Fig. 8(A), the electrically conductive layer (A) 801 is set to 10 to 100 nm (preferably 20 to 50 nm) in thickness, and the electrically conductive layer (B) 802 is set to 200 to 400 nm (preferably 250 to 350 nm) in thickness. For example, in the case where the W film is formed as the gate electrode, the electrically conductive layer (A) 801 is formed in thickness of 50 nm with a WN film and the electrically conductive layer (B) 802 is formed in thickness of 250 nm with a W film by introducing an Ar gas and nitrogen (N_2) gas through the sputtering method with W as a target. However, in order to employ the W film as the gate electrode, it is necessary to lower the resistance, and the resistivity is preferably set to 20 $\mu\Omega$cm or less. The W film can be lowered in resistivity by increasing crystal grains. However, in the case where a large amount of impurity elements such as oxygen are contained in W, crystallization is impeded to make the resistance high. For that reason, in the case of using the sputtering method, a W target with a purity of 99.9999%, and the W film is also formed while satisfactorily paying attention to the impurities being not mixed from a gas phase at the time of forming a film. In particular, it is better that the density of oxygen is set to 30 ppm or less. For example, W can realize the specific resistance of 20 $\mu\Omega$m or less when the density of oxygen is set to 30 ppm or less.

On the other hand, in Fig. 8A, in the case where a TaN film is used for the electrically conductive layer (A) 801, and a Ta film is used for the electrically conductive layer (B) 802, those films can be formed through the sputtering method likewise. The TaN film is formed using a mixture gas of Ar and nitrogen as a sputtering gas and Ta as a target, and the Ta film is formed by using Ar as the sputtering gas. Also, if an appropriate amount of Xe and Kr are added in those sputtering gases, the internal stress of a film to be formed is relieved, thereby being capable of preventing the films from being peeled off. The Ta film of an α-

phase is about 20 $\mu\Omega$cm in resistivity and can be used as the gate electrode, but the Ta film of a β-phase is about 180 $\mu\Omega$cm in resistivity and is improper as the gate electrode. Since the TaN film has the crystal structure close to the α-phase, if the Ta film is formed on the TaN film, the Ta film of the α-phase is readily obtained. In any cases, it is preferable that the electrically conductive layer (B) 802 is formed in the resistivity of 10 to 50 $\mu\Omega$cm.

In the case of the structure shown in Fig. 8B, the electrically conductive layer (A) 803 is set to 10 to 100 nm (preferably 20 to 50 nm) in thickness, the electrically conductive layer (B) 804 is set to 200 to 400 nm (preferably 250 to 350 nm) in thickness, and the electrically conductive layer (C) 805 is set to 10 to 100 nm (preferably 20 to 50 nm) in thickness. In this example, the electrically conductive layer (A) and the electrically conductive layer (C) are formed of a WN film or TaN film of the heat-resistant electrically conductive material, or a Ti film, a Ta film, a W film or the like as described above. The electrically conductive layer (B) 804 is also formed through the sputtering method and formed of 0.01 to 5 atomic% of Al film containing Ti, Si or the like in addition to pure Al.

The gate electrode 102, the gate wiring 102', the storage capacitor wiring 103 and the terminal 104 are formed by conducting a first photolithography process after formation of the electrically conductive layer on the entire substrate surface, forming a resist mask and removing an unnecessary portion by etching. In this situation, etching is conducted in such a manner that a tapered portion is formed on at least an end portion of the gate electrode 102.

In order to etch the heat-resistant electrically conductive material such as the W film or the Ta film at a high speed and with a high accuracy and to taper the end portion of the material, the dry etching method using the high-density plasma is proper. In order to obtain

the high-density plasma, an etching device using micro-waves or inductively coupled plasma (ICP) is proper. In particular, the ICP etching device is easy in the control of plasma and can be adapted to the large area of the substrate to be processed. For example, as the specific etching condition of the W film, the mixture gas of CF_4 and Cl_2 is used for the etching gas, their flow rates are 30 SCCM, respectively, the discharge power is 3.2 W/cm^2 (13.56 MHz), the substrate bias power is 224 mW/cm^2 (13.56 MHz), and the pressure is 1.0 Pa, under the conditions of which etching is conducted. Under the above conditions, the tapered portion that gradually increases its thickness inwardly from the end portion of the gate electrode 102 is formed at the end portion thereof, and the angle is set to 1 to 20°, more preferably 5 to 15°. As shown in Fig. 9, the angle of the tapered portion on the end portion of the gate electrode 102 is an angle of a portion indicated by Θ. The angle Θ of the tapered portion is represented by Tan (Θ) = HG/WG using the length (WG) of the tapered portion and the thickness (HG) of the tapered portion.

After the gate electrode 102, the gate wiring 102', the storage capacitor wiring 103 and the terminal 104 are formed, an insulating film is formed on the entire surface to provide a gate insulating layer. The gate insulating layer 105 is formed of an insulating film 50 to 200 nm in thickness through the plasma CVD method or the sputtering method. For example, the gate insulating film 105 is formed of a silicon nitrogen oxide film in thickness of 150 nm. Also, since the silicon nitrogen oxide film fabricated by adding O_2 to SiH_4 and N_2O is reduced in the fixed charge density in the film, it is a preferred material for this application. It is needless to say that the gate insulating layer is not limited to the above silicon nitrogen oxide film, but may be formed of a single layer or a lamination structure made of materials of other insulating films such as a silicon oxide film, a silicon nitride film and a tantalum oxide film.

For example, in the case of using the silicon oxide film, the gate insulating layer can be formed by mixing tetraethyl orthosilicate (TEOS) and O_2 together and conducting electric discharge at a high frequency (13.56 MHz) with a power density of 0.5 to 0.8 W/cm^2 under the conditions where the reactive pressure is 40 Pa and the substrate temperature is 250 to 350°C. The silicon oxide film thus fabricated can obtain an excellent characteristic as the gate insulating layer by thereafter thermally annealing the silicon oxide film at 300 to 400 °C.

Subsequently, a semiconductor layer having an amorphous structure is formed in thickness of 50 to 200 nm (preferably 100 to 150 nm) on the entire surface of the gate insulating layer through a known method such as the plasma CVD method or the sputtering method (not shown). Representatively, an amorphous silicon hydride (a-Si:H) film is formed in thickness of 100 nm through the plasma CVD method. The semiconductor layer having the amorphous structure may be formed of a compound semiconductor film having an amorphous structure such as a micro-crystal semiconductor film or an amorphous silicon germanium film. In addition, as a semiconductor layer containing one-conductive type impurity elements therein, an n-type semiconductor film is formed in thickness of 20 to 80 nm. For example, an n-type a-Si:H film may be formed, and in order to form the film, a phosphine (PH_3) 1 to 5% in density is added to silane (SiH_4). Alternatively, an n-type semiconductor film may be formed of a micro-crystal silicon hidride film (μc-Si:H).

The gate insulating film, the semiconductor layer having the amorphous structure and the semiconductor layer containing the one-conductive type impurity elements are fabricated by a known method, and may be fabricated by the plasma CVD method or the sputtering method. Those films can be sequentially formed by appropriately switching over the reactive gas if the plasma CVD method is applied, and by appropriately switching over the

target and the sputtering gas if the sputtering method is applied. That is, those films can be sequentially laminated without being exposed to the atmosphere by using the same reactive chamber or a plurality of reactive chambers in a plasma CVD device or a sputtering device.

The semiconductor layers thus laminated is patterned in a second photolithography process so that an island-like semiconductor layer is so formed as to be overlapped with the gate electrode 102. The island-like semiconductor layer has an amorphous semiconductor layer 106a and an n-type semiconductor layer 106b.

Then, an electrically conductive metal layer is formed through the sputtering method or the vacuum evaporation method, a resist mask pattern is formed in a third photolithography process, and a source wiring 107, a drain wiring 108 and a storage capacitor wiring 109 are formed by etching as shown in Fig. 2A. Although being not shown, in this embodiment, the wiring is formed in such a manner that a Ti film is formed in thickness of 50 to 150 nm, brought in contact with the n-type semiconductor film that forms the source or drain region of the island-like semiconductor layer, and aluminum (Al) is formed in thickness of 300 to 400 nm on the Ti film, and another Ti film is formed in thickness of 100 to 150 nm on the aluminum film.

Also, in an input terminal portion connected to the source wiring, a wiring 110 is formed on the gate insulating layer so as to positionally coincide with the input terminal portion. Although this appearance is omitted from Fig. 2A, the wiring 110 extends on the gate insulating layer and is connected to the source wiring.

Using a source wiring 107 and a drain wiring as masks, the n-type semiconductor layer 106b and the amorphous semiconductor layer 106a are partially removed by etching, to thereby form an aperture 111 in the island-like semiconductor layer as shown in the part (II)

of Fig. 2A. The aperture 111 allows the n-type semiconductor layer 106b to be divided into a source region 112 and a drain region 113, to thereby form a channel formation region in the island-like semiconductor layer 106 in a self-aligning manner.

Thereafter, as shown in the part (II) of Fig. 2B, a first interlayer insulating layer 114 made of an inorganic material which covers the aperture 111 and comes in contact with at least a part of the channel formation region is formed on the semiconductor layer having the amorphous structure and the n-type semiconductor layer. The first interlayer insulating layer 114 is formed of a silicon oxide film, a silicon nitrogen oxide film, a silicon nitride film or a lamination film combining those films together. The thickness of the first interlayer insulating film 114 is set to 100 to 200 nm. For example, in the case where the first interlayer insulating film 114 is formed of the silicon oxide film, the first interlayer insulating film 114 can be formed by mixing TEOS and O_2 together through the plasma CVD method and conducting electric discharge at a high frequency (13.56 MHz) with a power density of 0.5 to 0.8 W/cm^2 under the conditions where the reactive pressure is 40 Pa and the substrate temperature is 200 to 300°C. Also, in the case where the first interlayer insulating film 114 is formed of the silicon nitrogen oxide film, the first interlayer insulating film 114 may be formed of a silicon nitrogen oxide film fabricated by SiH_4, N_2O and NH_3 through the plasma CVD method or a silicon nitrogen oxide film fabricated by SiH_4 and N_2O through the plasma CVD method. In this example, the first interlayer insulating film 114 can be formed at a high frequency (60 MHz) with a power density of 0.1 to 1.0 W/cm^2 under the conditions where the reactive pressure is 20 to 200 Pa and the substrate temperature is 200 to 300°C. Also, a silicon nitrogen hydrogen oxide film made of SiH_4, N_2O and NH_3 may be applied to the first interlayer

insulating film 114. Similarly, the silicon nitride film can be fabricated by SiH_4 and NH_3 through the plasma CVD method.

In addition, a second interlayer insulating layer 115 made of an organic material and formed on the first interlayer insulating film 114 is formed in the average thickness of 1.0 to 2.0 μm. The organic resin material may be polyimide, acrylic, polyamide, polyimidamide, BCB (benzocyclobutene) or the like. For example, in the case of using polyimide of the type where the material is thermally polymerized after it is coated on a substrate, polyimide is baked by a clean oven at 200 to 300 °C to form the second interlayer insulating layer 115. Also, in the case of using acrylic, a two-liquid material is used, and after a main material and a curing agent are mixed together, the mixed material is coated on the entire surface of the substrate by using a spinner. Thereafter, the coated material is pre-heated by a hot plate at 80 °C for 60 seconds, and further baked by a clean oven at 180 to 250 °C for 60 minutes, thereby being capable of forming the second interlayer insulating layer 115.

Since the second interlayer insulating film 114 is made of the organic insulating material, the surface can be excellently flattened. Also, since the organic resin material is generally low in permittivity, a parasitic capacitor can be reduced. However, since the organic resin material has the hygroscopic property and not proper for a protective film, it is preferable that the second interlayer insulating film 115 is combined with the silicon oxide film, the silicon nitrogen oxide film, the silicon nitride film or the like formed as the first interlayer insulating film 114 as in this embodiment.

Thereafter, a fourth photolithography process is conducted to form a resist mask of a predetermined pattern, thereby forming contact holes that reaches the source region or the drain region which is defined in the respective island-like semiconductor layers. The contact

holes are formed through the dry etching method. In this case, the second interlayer insulating film 115 made of an organic resin material is first etched by using the mixture gas of CF_4, O_2 and He as an etching gas, and thereafter the first interlayer insulating film 114 is etched by using CF_4 and O_2 as an etching gas. On the input terminal portion, the second interlayer insulating film 115, the first interlayer insulating film 114 and the gate insulating layer 105 are partially etched so that the terminal 104 and the wiring 110 are partially exposed.

Then, a transparent electrically conductive film is formed in thickness of 50 to 200 nm through the sputtering method or the vapor evaporation method, and a fifth photolithography process is conducted to form a pixel electrode 118 as shown in Fig. 2B. The pixel electrode 118 is connected to the drain wiring 108 on a connecting portion 116 and also connected to the storage capacitor electrode 109 on a connecting portion 117. At the same time, a transparent electrically conductive film 119 is so disposed as to be in contact with at least parts of the terminal 104 and the wiring 110. The detail of a cross-sectional view of the section B-B' which is taken along a direction indicated by an arrow in the part (II) of Fig. 2B is shown in Fig. 11A. In the figure, the gate electrode 104 is formed of an electrically conductive layer (A) 130 and an electrically conductive layer (B) 131, and the transparent electrically conductive film 119 is so formed as to be in contact with at least parts of the electrically conductive layer (A) 130 and the electrically conductive layer (B) 131. Also, the detail of a cross-sectional view of the section C-C' which is taken along a direction indicated by an arrow in the part (II) of Fig. 2B is shown in Fig. 11B. The wiring 110 is of a three-layer structure consisting of a Ti film 132, an Al film 133 and a Ti film 134, and the transparent electrically conductive film 119 is so formed as to be in contact with at least parts of those films. In this way, the terminal 104 and the wiring 110 are electrically connected to each other.

However, it is unnecessary to dispose the wiring 110 on the input terminal portion which is connected to the gate wiring, and the transparent electrically conductive film 119 is so disposed as to be in contact with at least a part of the terminal 104.

The transparent electrically conductive film is formed of indium oxide (In_2O_3), an alloy of indium oxide and tin oxide (In_2O_3-SnO_2, ITO for short) or the like through the sputtering method, the vapor evaporation method or the like. The etching process of those materials is conducted by using the solution of hydrochloric acid. However, since the residue is liable to occur particularly in the etching of ITO, an alloy of indium oxide and tin oxide (In_2O_3-ZnO) may be used in order to improve the etching property. Since the alloy of indium oxide and tin oxide (In_2O_3-ZnO) is excellent in surface smoothness and also excellent in heat stability as compared with ITO, even if the terminal 104 is formed of an Al film, corrosion can be prevented. Similarly, zinc oxide (ZnO) is also a proper material, and further zinc oxide (ZnO:Ga) to which gallium (Ga) is added may be employed in order to enhance the transmittance of the visible light and the electric conductivity.

In this way, an inverse stagger type n-channel TFT 120 and a storage capacitor 121 can be completed through the five photolithography processes by using the five photomasks. Those TFTs 120 and capacities 121 are disposed in a matrix in correspondence with the respective pixels to form a pixel portion, thereby being capable of providing one substrate for manufacturing an active matrix liquid crystal display device. In the present specification, the above substrate is called "active matrix substrate" for convenience.

Fig. 10 is a diagram for explanation of an arrangement of a pixel portion and an input terminal portion of the active matrix substrate. A pixel portion 902 is disposed on a substrate 901, and gate wirings 908 and source wirings 907 are disposed on the pixel portion

so as to cross each other. The n-channel TFTs 910 which are connected to the gate wirings 908 and the source wirings 907 are disposed in correspondence with the respective pixels. The drain side of the n-channel TFT 910 is connected with one terminal of a storage capacitor 911, and another terminal of the storage capacitor 911 is connected to a storage capacitor wiring 909. The structures of the n-channel TFT 910 and the storage capacitor 911 are identical with those of the n-channel TFT 120 and the storage capacitor 121 shown in Fig. 2B.

One end portion of the substrate is formed with an input terminal portion 905 that inputs a scanning signal, and connected to the gate wiring 908 by a gate wiring 906. Also, another end portion of the substrate is formed with an input terminal portion 903 that inputs an image signal and connected to the source wirings 907 by the connecting wiring 904. The number of gate wirings 908, the number of source wirings 907 and the number of storage capacitor wirings 909 are plural in accordance with the pixel density, and their number is described above. Also, an input terminal portion 912 that inputs the image signal and a connecting wiring 913 may be disposed so that the source wirings are alternately connected to the input terminal portions 912 and 903. The numbers of input terminal portions 903, 905 and 912 may be arbitrarily set and may be appropriately determined by an implementor.

(Second Embodiment)

A description will be given of a method in which TFTs of the pixel portion are formed in the inverse stagger type on the substrate with a structure different from that in the first embodiment to manufacture the storage capacitor connected to the TFTs with reference to Figs. 3A to 4B. Similarly, in Figs. 3A, 3B and Figs. 4A, 4B, their parts (I) are top views and cross-sectional views taken along a line A-A' are shown by parts (II). The active matrix substrate manufactured by this embodiment corresponds to the transmission-type liquid crystal

display device, and hereinafter differences from the first embodiment will be mainly described.

Referring to Fig. 3A, a substrate 201 may be made of a glass substrate such as barium boro-silicate glass or alumino boro-silicate glass which is represented by #7059 glass or #1737 glass made by Corning Inc. Alternatively, a stainless substrate or a ceramic substrate on which an oxide silicon film a nitride silicon film or the like is formed on the surface may be employed as the substrate 201.

A gate electrode 202, a gate wiring 202', a storage capacitor wiring 203 and a terminal 204 of an input terminal portion may be desirably made of the combination of a low-resistive wiring material such as Al with a heat-resistant electrically conductive material. Alternatively, they may be made of the combination of only the heat-resistant electrically conductive materials. For example, a lamination structure of a WN film and a W film may be applied. After the electrically conductive layer with the above structure has been formed on the entire surface of the substrate, a first photolithography process is conducted to form a resist mask, and unnecessary portions are removed by etching to form those components. In this situation, etching is conducted so that a tapered portion is formed on at least an end portion of the gate electrode 202.

The gate insulating layer 205 is formed of a silicon oxide film, a silicon nitrogen oxide film, a silicon nitride film, a tantalum oxide film or the like in the thickness of 50 to 200 nm through the plasma CVD method or the sputtering method. Subsequently, a semiconductor layer having an amorphous structure is formed in thickness of 50 to 200 nm (preferably 100 to 150 nm) on the entire surface of the gate insulating layer 205 through a known method such as the plasma CVD method or the sputtering method (not shown). Representatively, an

amorphous silicon hydride (a-Si:H) film is formed through the plasma CVD method. In addition, as a semiconductor layer containing one-conductive type impurity elements therein, an n-type semiconductor film is formed in thickness of 20 to 80 nm. For example, an n-type a-Si:H film may be formed.

Then, a second photolithography process is conducted on the semiconductor layer thus laminated and formed, and an island-like semiconductor layer 206 is so formed as to be overlapped with the gate electrode 202 as shown in Fig. 2B. The island-like semiconductor layer 206 has an amorphous semiconductor layer 206a and an n-type semiconductor layer 206b.

Subsequently, as shown in the part (II) of Fig. 4A, a third photolithography process is conducted to remove a part of the gate insulating film formed on the terminal 204 by etching, thereby defining an aperture 217. Then, the transparent electrically conductive film is formed in thickness of 50 to 200 nm through the sputtering method, the vapor evaporation method, the spray method or the like, and a transparent electrically conductive film 208 is formed on the pixel electrode 207 and the terminal 217 through a fourth photolithography process.

Thereafter, as in the first embodiment, an electrically conductive layer is formed through the sputtering method or the vapor evaporation method, a resist mask pattern is formed through a fifth photolithography process, and a source wiring 209 and a drain wiring 210 are formed by etching as shown in Fig. 4A. The drain wiring 210 is so formed as to be overlapped with the pixel electrode 207 on its end portion where the drain wiring 210 and the pixel electrode 207 are electrically connected to each other. Also, the connection of the source wiring with the input terminal portion is made such that an end portion 211 of the source

wiring extending on the gate insulating film is so formed as to be overlapped with the transparent electrically conductive film 208 and electrically connected to the terminal 204.

The n-type semiconductor layer 206b and the amorphous semiconductor layer 206a are partially removed by etching with the source wiring 209 and the drain wiring 210 as masks, to thereby form an aperture 212 in the island-like semiconductor layer as shown in the part (II) of Fig. 4B. The aperture 212 allows the n-type semiconductor layer 206b to be divided into a source region 213 and a drain region 214, to thereby form a channel formation region in the island-like semiconductor layer 206 in a self-aligning manner.

Thereafter, as shown in the part (II) of Fig. 4B, a first interlayer insulating layer 215 made of an inorganic material which covers the aperture 212 and comes in contact with at least a part of the channel formation region is formed on the semiconductor layer having the amorphous structure and the n-type semiconductor layer. The first interlayer insulating film 215 is formed of a silicon oxide film, a silicon nitrogen oxide film, a silicon nitride film or a lamination film combining those films together. The thickness of the first interlayer insulating film 215 is set to 100 to 200 nm. Then, the first interlayer insulating layer 215 on the pixel electrode 207 and the transparent electrically conductive film 208 of the input terminal portion is removed through a sixth photolithography process.

In this way, an inverse stagger type n-channel TFT 220 and a storage capacitor 221 can be completed through the six photolithography processes by using the six photomasks. The arrangement of the pixel portion and the input terminal portion in the active matrix substrate manufactured in accordance with this embodiment is identical with that in the first embodiment as shown in Fig. 10.

(Third Embodiment)

The second embodiment shows a method of manufacturing an active matrix substrate adaptive to the transmission type liquid crystal display device, and a third embodiment shows an example adaptive to a reflection type liquid crystal display device.

First, the processes shown in Fig. 3B are conducted in the same manner as that in the second embodiment. Then, as shown in the part (II) of Fig. 5, a third photolithography process is conducted to remove a part of the gate insulating film disposed on the terminal 204 by etching, to thereby form an aperture 230. Then, an electrically conductive layer is formed through the sputtering method and the vapor evaporation method as in the first embodiment, a resist mask pattern is formed through a fourth photolithography process, and a source wiring 231 and a drain wiring 232 are formed by etching as shown in Fig. 5. The drain wiring 32 serves as a pixel electrode and is so formed as to be overlapped with the storage capacitor wiring 203. Also, the connection of the source wiring to the input terminal portion is made by electric connection with the terminal 204 in the aperture 230.

Thereafter, the first interlayer insulating layer 234 made of an organic material is formed as in the second embodiment. The first interlayer insulating layer 234 on the pixel electrode and the input terminal portion is removed through a fifth photolithography process. In this way, an active matrix substrate adaptive to the reflection type liquid crystal display device can be fabricated by using five photomasks through the five photolithography process.

(Fourth Embodiment)

In a fourth embodiment, a description will be given of a process of fabricating an active matrix liquid crystal display device from the active matrix substrate fabricated in the first embodiment. As shown in Fig. 6, an oriented film 600 is formed on an active matrix

substrate which is in a state shown in Fig. 2B. Normally, the oriented film of the liquid crystal display device is frequently made of polyimide resin.

A light shielding film 602, a color filter 603 and a flattening film 604, a transparent electrically conductive film 605 and an oriented film 606 are formed on a counter substrate 601 opposite to the oriented film 600. The light shielding film 602 is made of Ti, Al, chrome (Cr) or the like and patterned in accordance with the arrangement of TFTs of the active matrix substrate. Color filters 603 consisting of red, green and blue filters are disposed in correspondence with the respective pixels. The flattening film 604 is formed of an organic resin film and may be made of the same material as that of the second interlayer insulating film used in the first embodiment. After the oriented film has been formed, liquid crystal molecules are subjected to a rubbing process so as to be oriented with a given pre-tilted angle.

Then, the active matrix substrate on which the pixel portion is formed and the counter substrate are bonded together through a spacer 607 by a sealant 608 containing a spacer 609 therein through a known cell assembling process. As a result, a liquid crystal injection region 610 is formed. The liquid crystal material may be a known material and representatively TN liquid crystal. After the injection of the liquid crystal material, an injection port is sealed with a resin material. In case of the transmission type liquid crystal display device, polarizing plates 611 and 612 are bonded together to complete an active matrix liquid crystal display device shown in Fig. 6. In case of the reflection type liquid crystal display device, the polarizing plate 612 is omitted, and the polarizing plate 611 is disposed on only the counter substrate 601 side.

This embodiment shows a method of manufacturing an active matrix liquid crystal display device on the basis of the active matrix substrate fabricated in the first embodiment.

However, the active matrix liquid crystal display device can be fabricated in the same manner even if the active matrix substrate shown in the second or third embodiment is employed.

(Fifth Embodiment)

The active matrix substrate and the liquid crystal display device which are manufactured by implementing the present invention can be applied to various electro-optic devices. Then, the present invention is applicable to all the electronic devices installed with the electro-optic device as a display medium. The electronic device includes a personal computer, a digital camera, a video camera, a portable information terminal (a mobile computer, a portable telephone, an electronic document, etc.,), a television, etc.

Fig. 12A shows a personal computer which is made up of a main body 2001 with a microprocessor, a memory and so on, an image input section 2002, a display device 2003 and a key board 2004. The present invention is applicable to the display device 2003.

Fig. 12B shows a video camera which is made up of a main body 2101, a display device 2102, a voice input section 2103, an operating switch 2104, a battery 2105 and an image receiving section 2106. The present invention is applicable to the display device 2102.

Fig. 12C shows a portable information terminal which is made up of a main body 2201, an image input device 2202, an image receiving section 2203, an operating switch 2204 and a display device 2205. The present invention is applicable to the display device 2205.

Fig. 12C shows an electronic play device such as a TV game or a video game, which is made up of an electronic circuit 2308 such as a CPU, a main body 2301 on which a recording medium 2304 is mounted, a controller 2305, a display device 2303, a speaker 2307 and a display device 2302 installed in the main body 2301. The display device 2303 and the

display device 2302 installed in the main body 2301 may display the same information, or the former may serve as a main display device whereas the latter may serve as an auxiliary display device so as to display the information of the recording medium 2304, to display the operating state of the device, or provided with the function of a touch sensor to function as an operating board. Also, in order to mutually transmit a signal among the main body 2301, the controller 2305 and the display device 2303, wire communication may be conducted, or wireless communication or optic communication may be conducted with the provision of sensor portions 2306 and 2307. The display device 2303 enables its screen size to increase up to about 30 inches, and can be employed as a television in combination with a tuner not shown.

Fig. 12D shows a player using a recording medium in which program has been recorded (hereinafter referred to as "recording medium") which is made up of a main body 2401, a display device 2402, a speaker portion 2403, a recording medium 2404 and an operating switch 2405. The recording medium may be formed of a DVD (digital versatile disc), a compact disc (CD) or the like so as to conduct the reproduction or an image display of a music program,, a video game (or TV game), or information display through the internet, etc. The present invention is preferably applicable to the display device 2402 or other signal control circuits.

Fig. 12E shows a digital camera which is made up of a main body 2501, a display device 2502, an eye-piece portion 2503, an operating switch 2504 and an image receiving portion (not shown). The present invention is applicable to the display device 2502 and other signal control circuits.

Fig. 7 shows an example of a method of mounting the above liquid crystal display device loaded on the electro-optic device. The liquid crystal display device is formed with an input terminal portion 702 on an end portion of a substrate 701 on which TFTs are manufactured, which is formed a terminal 703a made of the same material as that of the gate wiring as described in the first embodiment and a transparent electrically conductive film 703b. Then, the substrate 701 is bonded to a counter substrate 704 with a sealant 705 containing a spacer 706 therein, and polarizing plates 707 and 708 are further disposed. The bonded substrate is fixed to a casing 721 with a spacer 722.

A driving circuit is formed in an LSI chip 713 and mounted in the TAB system. The driving circuit is formed of a flexible printed circuit (FPC), and FPC is produced by forming a copper wiring 710 in an organic resin film 709 such as polyimide and connected to an input terminal 702 with an anisotropic electrically conductive agent. The anisotropic electrically conductive agent is made up of an adhesive 711 and particles 712 having an electrically conductive surface several tens to several hundreds μm in diameter, which are mixed in the adhesive 711 and plated with gold or the like. The particles 712 are brought in contact with the input terminal 702 and the copper wiring 710 where electric contact is formed. In order to enhance the mechanical strength of that portion, a resin layer 718 is formed.

The LSI chip 713 is connected to the copper wiring 710 with a bump 714 and sealed with a resin material 715. Then the copper wiring 710 is connected to a printed substrate 717 on which a signal processing circuit, an amplifier circuit, a power supply circuit and so on are disposed on a connecting terminal 716. In the transmission type liquid crystal display device, a light source 719 and an optically conductive member 720 are disposed on the counter substrate 704 and used as back-light.

Although being not shown in the above examples, the present invention is applicable to a navigation system, a portable television, and so on. As described above, the present invention is very widely applied and applicable to the electronic devices in any fields. The above electronic devices of this embodiment can be realized by using the techniques of the first to fourth embodiments.

The foregoing description of the preferred embodiments of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and modifications and variations are possible in light of the above teachings or may be acquired from practice of the invention. The embodiments were chosen and described in order to explain the principles of the invention and its practical application to enable one skilled in the art to utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto, and their equivalents.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate having an insulating surface;

a thin film transistor formed over the substrate, said thin film transistor comprising a channel formation region comprising a semiconductor layer having an amorphous structure; source and drain regions comprising a semiconductor layer including one conductive type impurity elements, and interposed between said substrate and said semiconductor layer having the amorphous structure;

a first interlayer insulating layer comprising an inorganic material and formed over said TFT wherein said first interlayer insulating layer is in contact with at least a part of the channel formation region;

a second interlayer insulating layer comprising an organic material and formed on the first interlayer insulating layer; and

a pixel electrode formed in contact with the second interlayer insulating layer.

2. A semiconductor device having over a substrate having an insulating surface a thin film transistor with a channel formation region formed of a semiconductor layer having an amorphous structure, a source region and a drain region each formed of a semiconductor layer containing one-conductive type impurity elements therein, and a gate electrode formed between the semiconductor layer having the amorphous structure and the substrate, the semiconductor device comprising:

a first interlayer insulating layer comprising an inorganic material and formed on the semiconductor layer having the amorphous structure and the semiconductor layer

containing the one-conductive type impurity elements so as to be in contact with at least a part of the channel formation region;

a second interlayer insulating layer comprising an organic material and formed on the first interlayer insulating layer;

a pixel electrode formed in contact with the second interlayer insulating layer; and

an input terminal portion formed along an end portion of the substrate and electrically connected to a wiring of another substrate;

wherein the input terminal portion includes a first layer comprising the same material as that of the gate electrode and a second layer comprising the same material as that of the pixel electrode.

3. A semiconductor device having over a substrate having an insulating surface a thin film transistor with a channel formation region formed of a semiconductor layer having an amorphous structure, a source region and a drain region each formed of a semiconductor layer containing one-conductive type impurity elements therein, a gate electrode formed between the semiconductor layer having the amorphous structure and the substrate, and an insulating layer formed on the gate electrode, the semiconductor device comprising:

an interlayer insulating layer comprising an inorganic material and formed on the semiconductor layer having the amorphous structure and the semiconductor layer containing the one-conductive type impurity elements so as to be in contact with at least a part of the channel formation region;

a pixel electrode formed in contact with the insulating layer; and

an input terminal portion formed along an end portion of the substrate and electrically connected to a wiring of another substrate;

wherein the input terminal portion includes a first layer comprising the same material as that of the gate electrode and a second layer comprising the same material as that of the pixel electrode.

4. A semiconductor device as claimed in claim 1 , wherein the gate electrode is comprising a heat-resistant electrically conductive material, or the heat-resistant electrically conductive material and a low-resistive electrically conductive material.

5. A semiconductor device as claimed in claim 2 , wherein the gate electrode is comprising a heat-resistant electrically conductive material, or the heat-resistant electrically conductive material and a low-resistive electrically conductive material.

6. A semiconductor device as claimed in claim 3, wherein the gate electrode is comprising a heat-resistant electrically conductive material, or the heat-resistant electrically conductive material and a low-resistive electrically conductive material.

7. A semiconductor device as claimed in claim 4, wherein the heat-resistant electrically conductive material is comprising an element selected from titanium (Ti), tantalum (Ta) or tungsten (W), a compound that contains any one of the above elements, a compound

film that combines the above elements together, or a nitride that contains any one of the above elements; and

wherein the low-resistive electrically conductive material is comprising a material containing aluminum (Al).

8. A semiconductor device as claimed in claim 5, wherein the heat-resistant electrically conductive material is comprising an element selected from titanium (Ti), tantalum (Ta) or tungsten (W), a compound that contains any one of the above elements, a compound film that combines the above elements together, or a nitride that contains any one of the above elements; and

wherein the low-resistive electrically conductive material is comprising a material containing aluminum (Al).

9. A semiconductor device as claimed in claim 6, wherein the heat-resistant electrically conductive material is comprising an element selected from titanium (Ti), tantalum (Ta) or tungsten (W), a compound that contains any one of the above elements, a compound film that combines the above elements together, or a nitride that contains any one of the above elements; and

wherein the low-resistive electrically conductive material is comprising a material containing aluminum (Al).

10. A semiconductor device as claimed in claim 1, wherein the semiconductor device comprises one of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disc player, an electronic play device and a television.

11. A semiconductor device as claimed in claim 2, wherein the semiconductor device comprises one of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disc player, an electronic play device and a television.

12. A semiconductor device as claimed in claim 3, wherein the semiconductor device comprises one of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disc player, an electronic play device and a television.

13. A method of manufacturing a semiconductor device, the method comprising:

a first step of forming a gate electrode over a substrate having an insulating surface;

a second step of forming a gate insulating layer on the gate electrode;

a third step of forming a semiconductor layer having an amorphous structure on the gate insulating layer;

a fourth step of forming a semiconductor layer containing a one-conductive type impurities on a semiconductor layer having the amorphous structure;

a fifth step of forming a source wiring and a drain wiring in contact with the semiconductor layer containing the one-conductive type impurities;

a sixth step of removing a pars of the semiconductor layer having the one-conductive type impurities and the semiconductor layer having the amorphous structure with the source wiring and the drain wiring as masks;

a seventh step of forming a first interlayer insulating layer comprising an inorganic material on the source wiring and the drain wiring;

an eighth step of forming a second interlayer insulating layer comprising an organic material on the first interlayer insulating layer; and

a ninth step of forming a pixel electrode on the second interlayer insulating layer.

14. A method of manufacturing a semiconductor device, comprising:

a first step of forming a gate electrode and a first layer of an input terminal portion which is electrically connected to a wiring on another substrate over a substrate having an insulating surface;

a second step of forming a gate insulating layer on the gate electrode;

a third step of forming a semiconductor layer having an amorphous structure on the gate insulating layer;

a fourth step of forming a semiconductor layer containing one-conductive type impurities therein on the semiconductor layer having the amorphous structure;

a fifth step of forming a source wiring and a drain wiring in contact with the semiconductor layer containing the one-conductive type impurities;

a sixth step of removing a part of the semiconductor layer containing the one-conductive type impurities and the semiconductor layer having the amorphous structure with the source wiring and the drain wiring as masks;

a seventh step of forming a first interlayer insulating layer comprising an inorganic material on the source wiring and the drain wiring;

an eighth step of forming a second interlayer insulating layer comprising an organic material on the first interlayer insulating layer;

a ninth step of selectively removing the first interlayer insulating layer, the second interlayer insulating layer and the gate insulating layer to expose the first layer of the input terminal portion; and

a tenth step of forming a pixel electrode and a second layer of the input terminal portion on the second interlayer insulating film.

15. A method of manufacturing a semiconductor device, comprising:

a first step of forming a gate electrode and a first layer of an input terminal portion which is electrically connected to a wiring on another substrate over a substrate having an insulating surface;

a second step of forming a gate insulating layer on the gate electrode;

a third step of forming a semiconductor layer having an amorphous structure on the gate insulating layer;

a fourth step of forming a semiconductor layer containing one-conductive type impurities therein on the semiconductor layer having the amorphous structure;

a fifth step of selectively removing the gate insulating layer to expose the first layer of the input terminal portion;

a sixth step of forming a pixel electrode and a second layer of the input terminal portion in contact with the gate insulating layer;

a seventh step of forming a source wiring and a drain wiring in contact with the semiconductor layer containing the one-conductive type impurities;

an eighth step of removing a part of the semiconductor layer containing the one-conductive type impurities and the semiconductor layer having the amorphous structure with the source wiring and the drain wiring as masks; and

a ninth step of forming a first interlayer insulating layer comprising an inorganic material on the source wiring and the drain wiring.

16. A method of manufacturing a semiconductor device as claimed in claim 13, wherein the gate electrode is comprising a heat-resistant electrically conductive material, or the heat-resistant electrically conductive material and a low-resistive electrically conductive material.

17. A method of manufacturing a semiconductor device as claimed in claim 14, wherein the gate electrode is comprising a heat-resistant electrically conductive material, or the heat-resistant electrically conductive material and a low-resistive electrically conductive material.

18. A method of manufacturing a semiconductor device as claimed in claim 15, wherein the gate electrode is comprising a heat-resistant electrically conductive material,

or the heat-resistant electrically conductive material and a low-resistive electrically conductive material.

19. A method of manufacturing a semiconductor device as claimed in claim 16, wherein the heat-resistant electrically conductive material is comprising an element selected from titanium (Ti), tantalum (Ta) or tungsten (W), a compound that contains any one of the above elements, a compound film that combines the above elements together, or a nitride that contains any one of the above elements; and

wherein the low-resistive electrically conductive material is comprising a material containing aluminum (Al).

20. A method of manufacturing a semiconductor device as claimed in claim 17, wherein the heat-resistant electrically conductive material is comprising an element selected from titanium (Ti), tantalum (Ta) or tungsten (W), a compound that contains any one of the above elements, a compound film that combines the above elements together, or a nitride that contains any one of the above elements; and

wherein the low-resistive electrically conductive material is comprising a material containing aluminum (Al).

21. A method of manufacturing a semiconductor device as claimed in claim 18, wherein the heat-resistant electrically conductive material is comprising an element selected from titanium (Ti), tantalum (Ta) or tungsten (W), a compound that contains any one of the above elements, a compound film that combines the above elements together, or a nitride that contains any one of the above elements; and

wherein the low-resistive electrically conductive material is comprising a material containing aluminum (Al).

22. A method of manufacturing a semiconductor device as claimed in claim 13, wherein the semiconductor device comprises one of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disc player, an electronic play device and a television.

23. A method of manufacturing a semiconductor device as claimed in claim 14, wherein the semiconductor device comprises one of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disc player, an electronic play device and a television.

24. A method of manufacturing a semiconductor device as claimed in claim 15, wherein the semiconductor device comprises one of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disc player, an electronic play device and a television.

ABSTRACT OF THE DISCLOSURE

In a semiconductor device, a first interlayer insulating layer made of an inorganic material and formed on inverse stagger type TFTs, a second interlayer insulating layer made of an organic material and formed on the first interlayer insulating layer, and a pixel electrode formed in contact with the second interlayer insulating layer are disposed on a substrate, and an input terminal portion that is electrically connected to a wiring of another substrate is provided on an end portion of the substrate. The input terminal portion includes a first layer made of the same material as that of the gate electrode and a second layer made of the same material as that of the pixel electrode. With this structure, the number of photomasks used in the photolithography method can be reduced to 5.

FIG. 1A

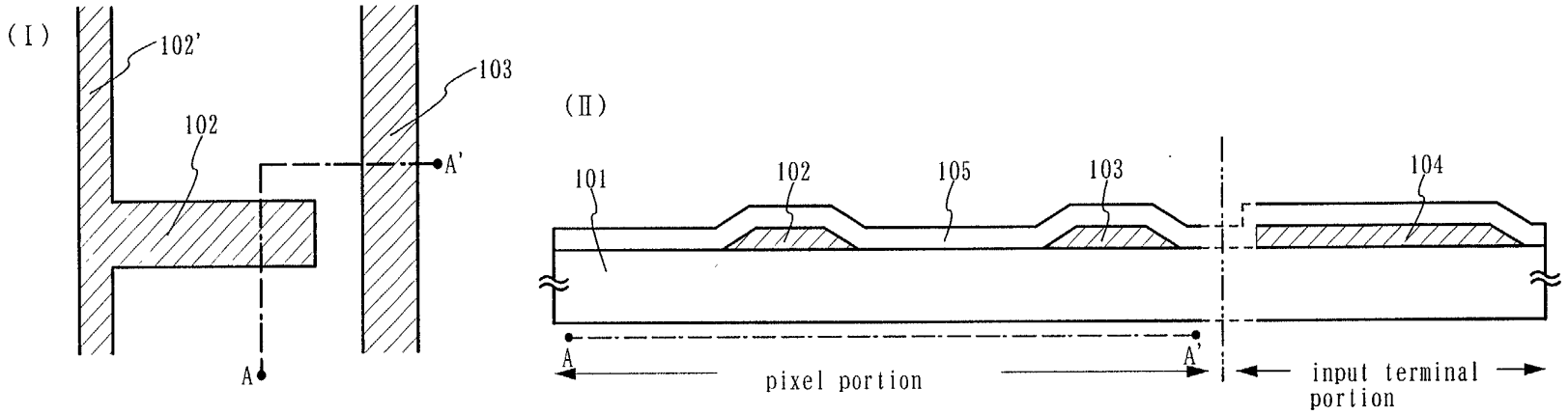

(I)
102'
103
102
A'
A
(II)
101
102
105
103
104
A
A'
pixel portion
input terminal portion

FIG. 1B

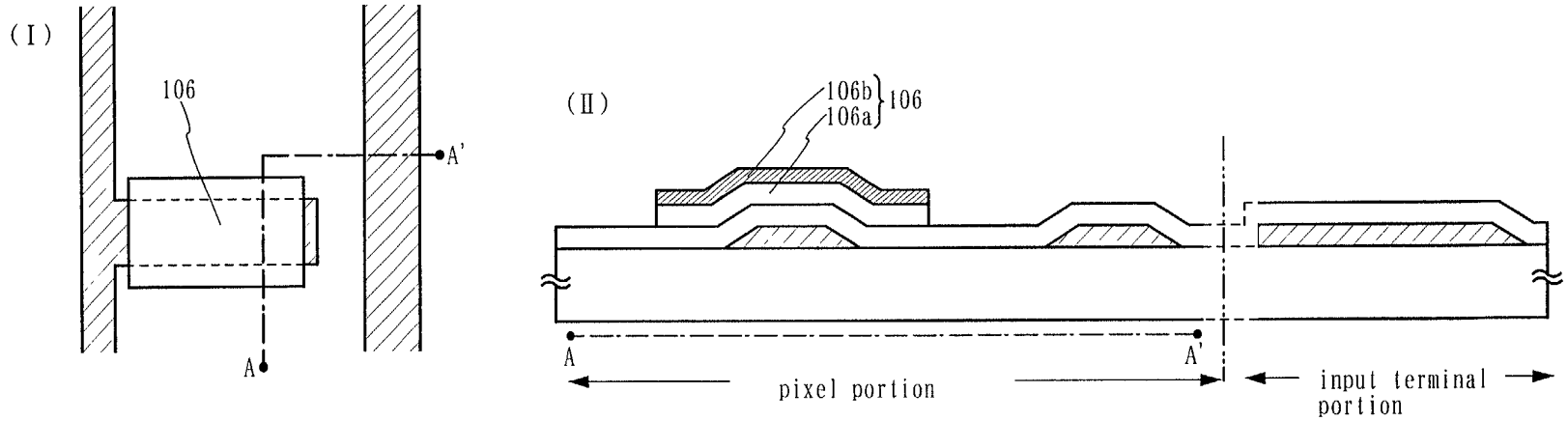

(I)
106
A'
A
(II)
106b
106a
106
A
A'
pixel portion
input terminal portion

FIG. 2A

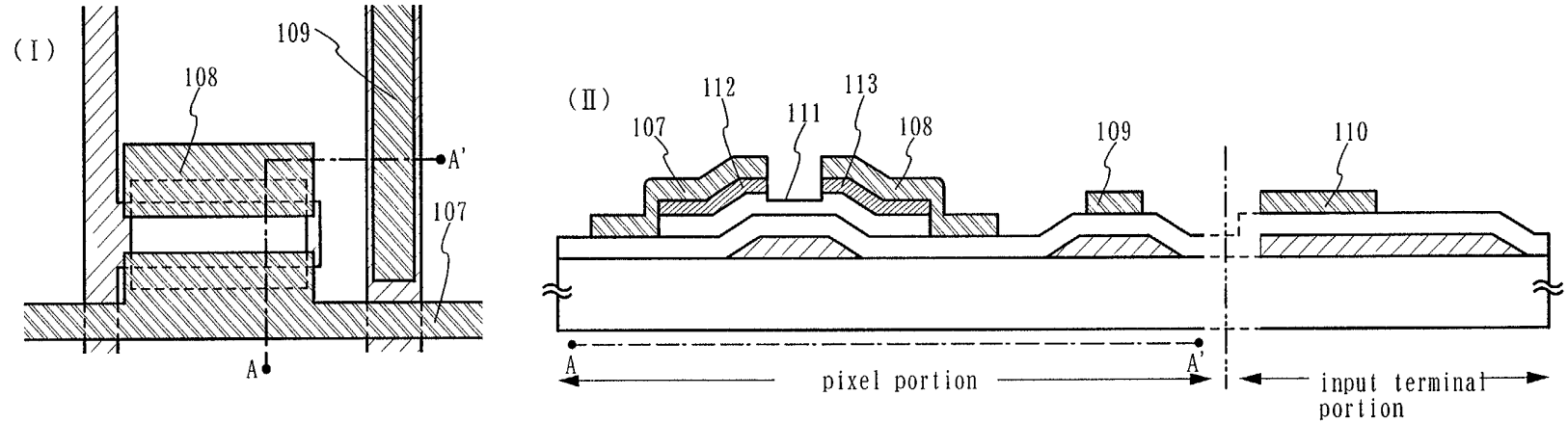

(I)
109
108
A'
107
A
(II)
112
113
111
107
108
109
110
A
A'
pixel portion
input terminal portion

FIG. 2B

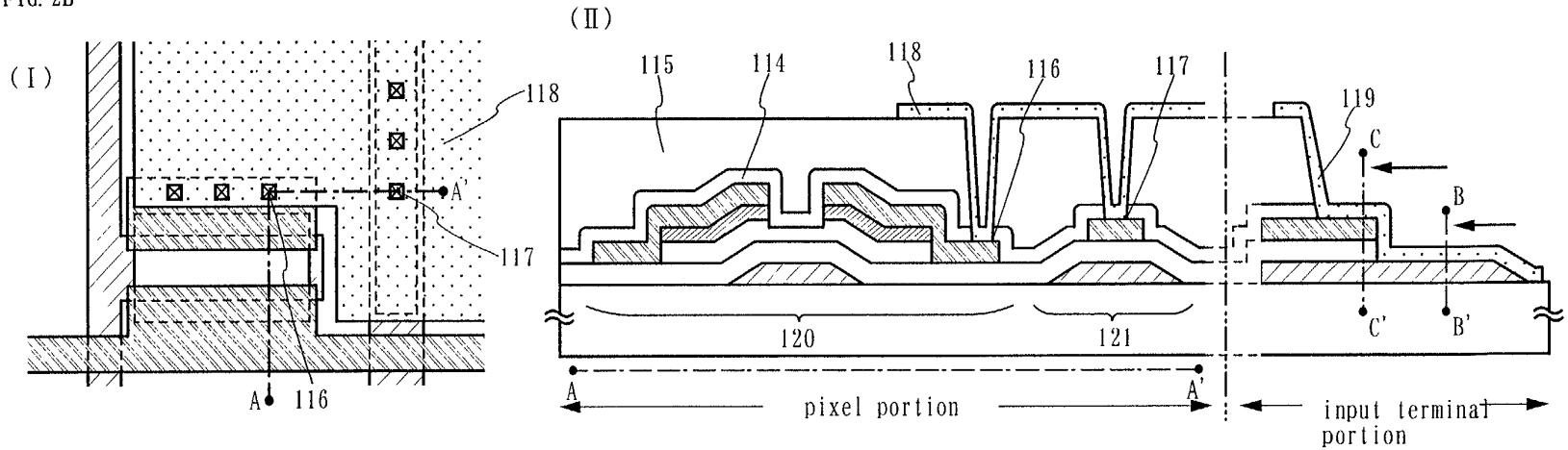

(I)
118
A'
117
A
116
(II)
115
114
118
116
117
119
C
B
C'
B'
120
121
A
A'
pixel portion
input terminal portion

FIG. 3A

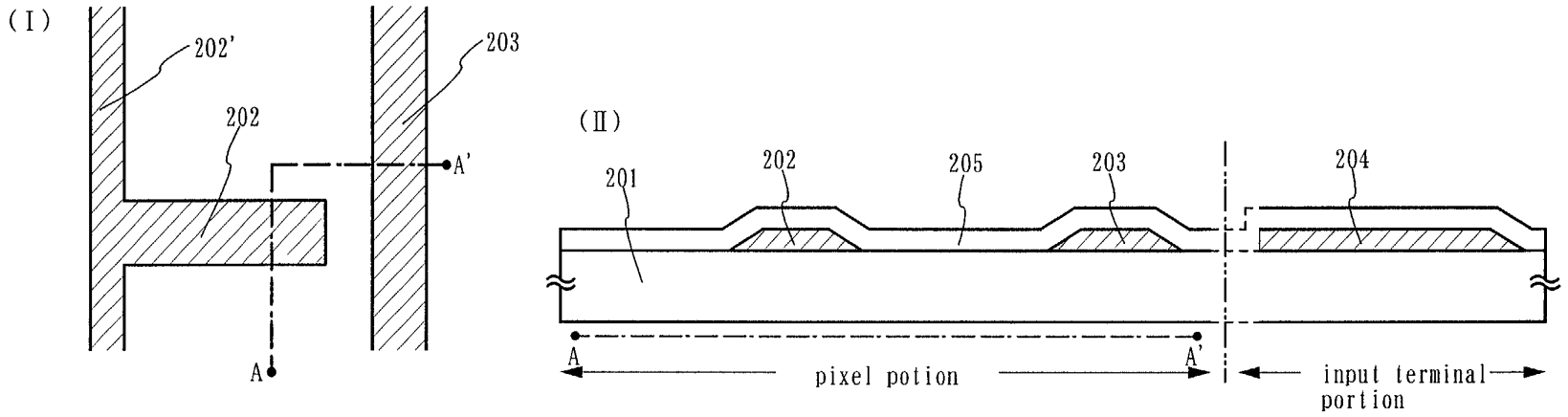


FIG. 3B

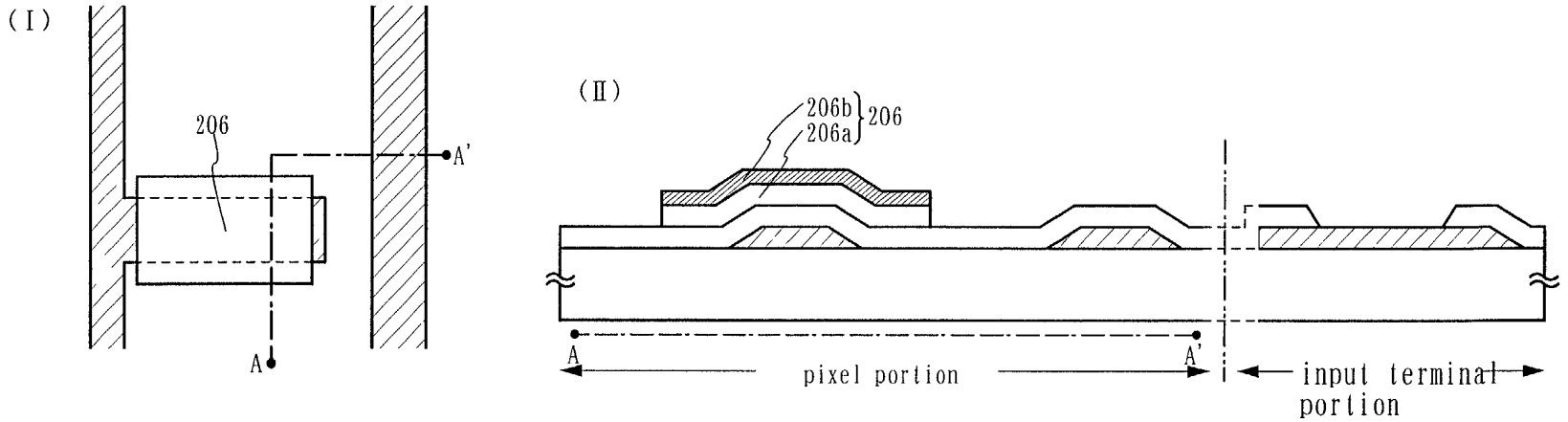


FIG. 4A

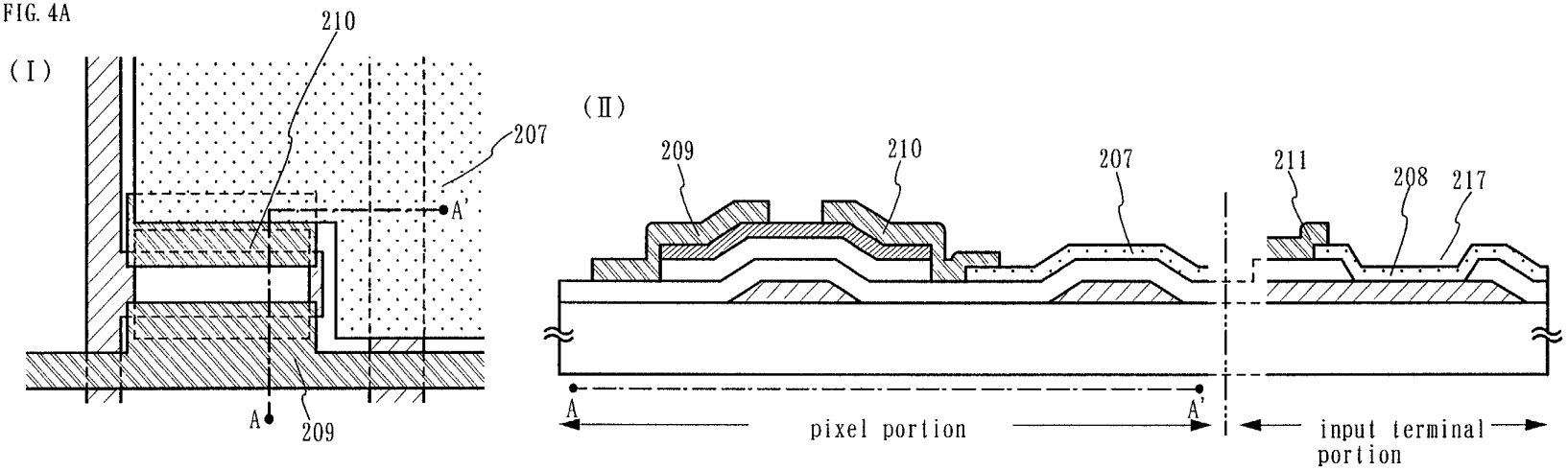
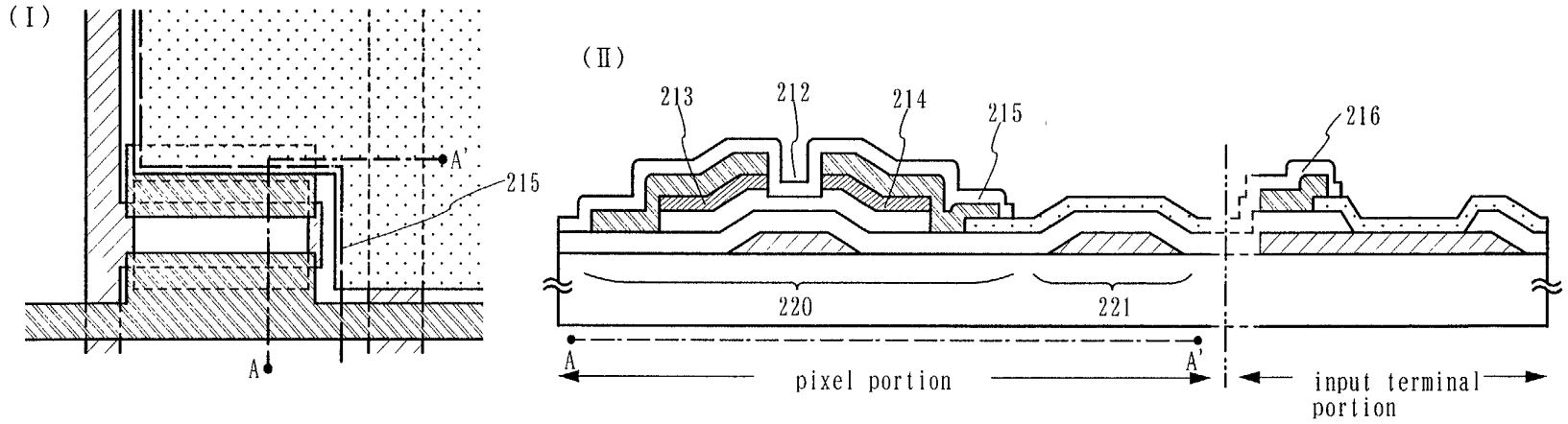

(I)
210
207
A'
A
209
(II)
209
210
207
211
208
217
A
A'
pixel portion
input terminal portion

FIG. 4B


(I)
A'
215
A
(II)
213
212
214
215
216
220
221
A
A'
pixel portion
input terminal portion

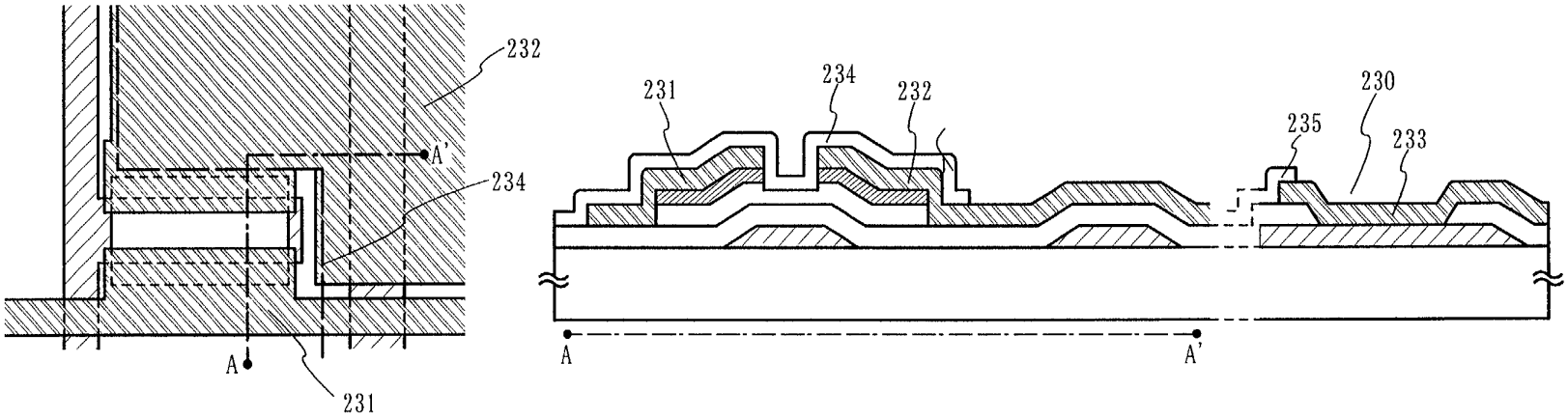


FIG. 5

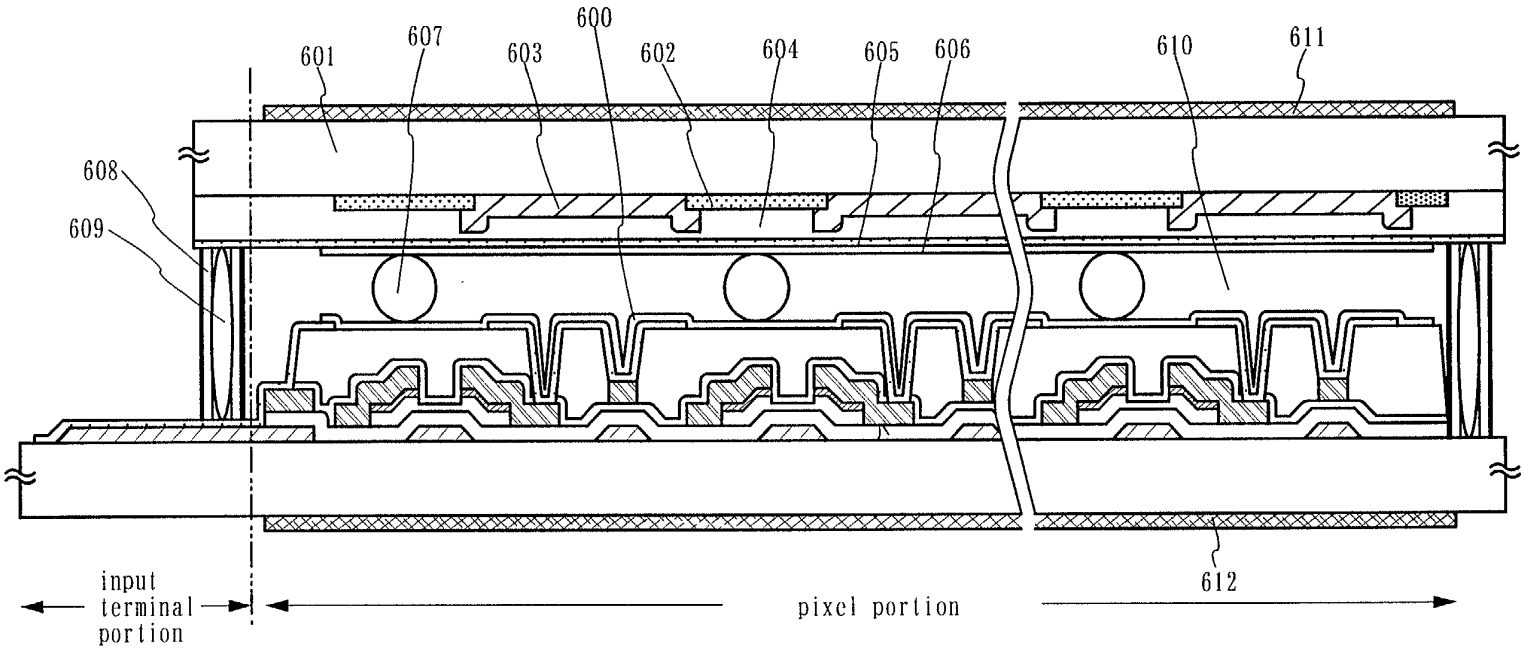

600
601
607
603
602
604
605
606
610
611
608
609
612
input terminal portion
pixel portion

FIG. 6

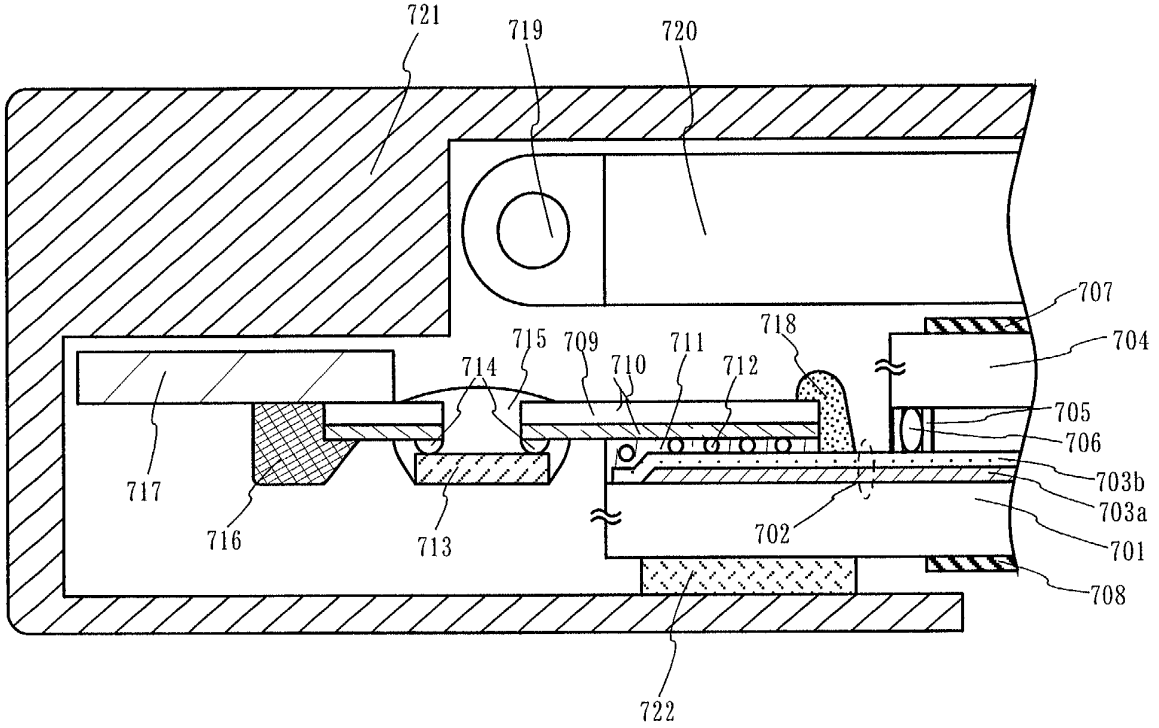

721
719
720
707
704
718
715
709
711
714
710
712
705
706
703b
703a
717
716
713
702
701
708
722

FIG. 7

FIG. 8A

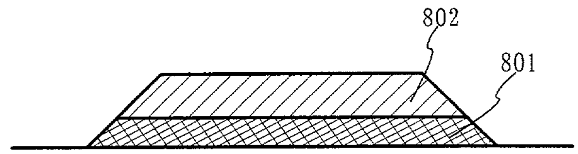
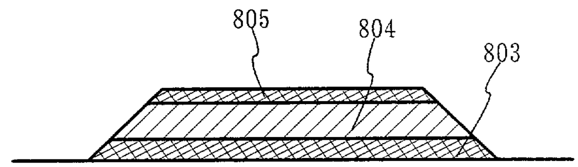


FIG. 8B



θ : angle of taper portion

FIG. 9

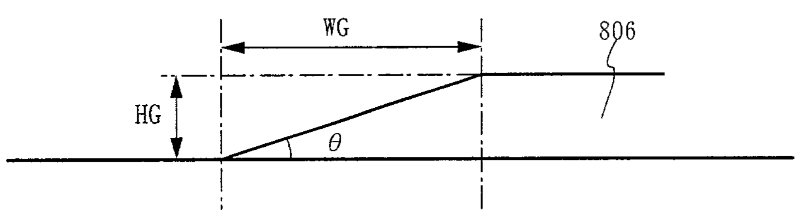


FIG. 10

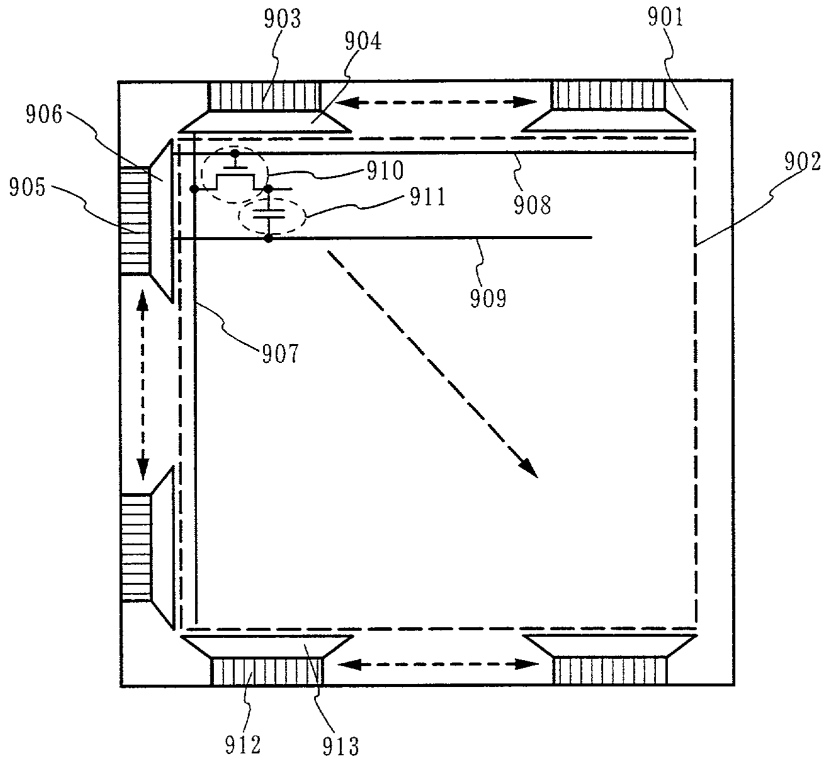


FIG. 11A

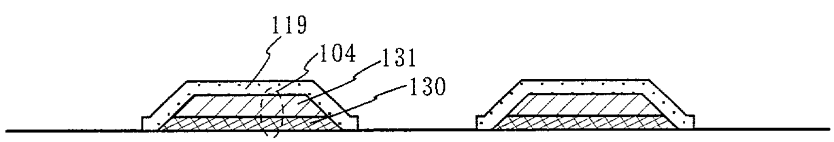
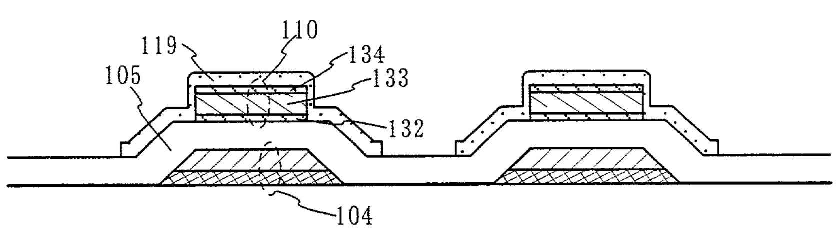


FIG. 11B



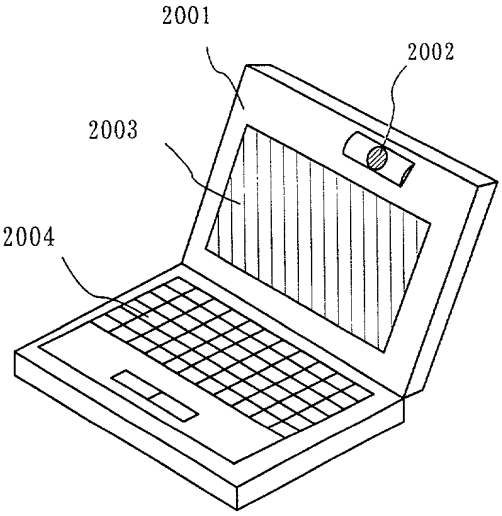


FIG. 12A

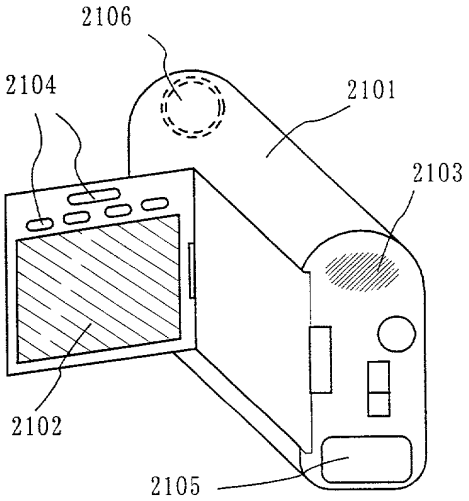


FIG. 12B

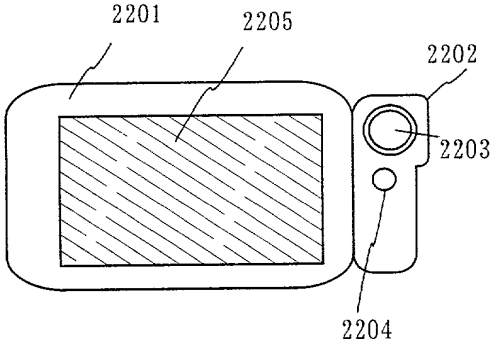


FIG. 12C

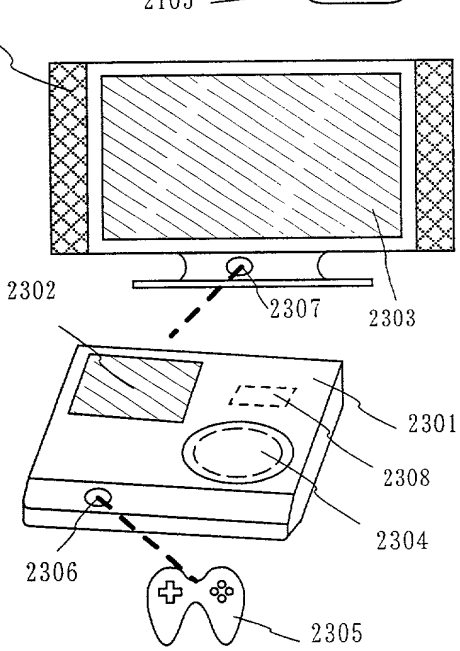


FIG. 12D

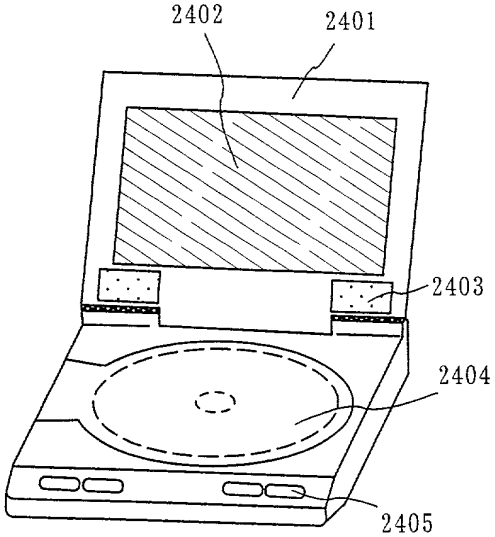


FIG. 12E

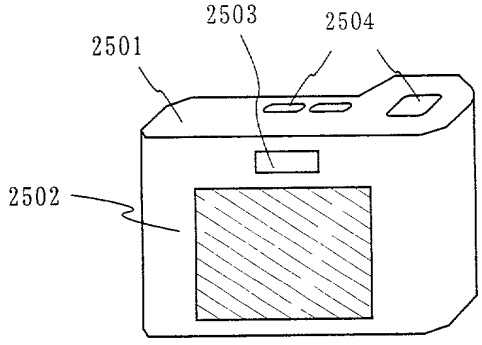


FIG. 12F

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration
日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

____

____

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SEMICONDUCTOR DEVICE

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

The specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を＿＿＿＿＿＿とし、（該当する場合）＿＿＿＿＿に訂正されました。

☐ was filed on ________________ as United States Application Number or PCT International Application Number ______________ and was amended on ________________ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基き下記の、米国以外の国の少なくとも一カ国を指定している特許協力条約 365(a)項に基く国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

Priority Not Claimed
優先権主張なし

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	
11-228944	Japan	August 12, 1999	☐
			☐
			☐

私は、第35編米国法典119条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第35編120条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約 365 条(c)に基く権利をここに主張します。また、本出願の各請求範囲の内容が米国法典代35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規制法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況: 特許許可済、継続中、放棄済)

(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況： 特許許可済、継続中、放棄済）
(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況： 特許許可済、継続中、放棄済）
(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況： 特許許可済、継続中、放棄済）
(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況： 特許許可済、継続中、放棄済）
(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況： 特許許可済、継続中、放棄済）
(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況： 特許許可済、継続中、放棄済）
(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況： 特許許可済、継続中、放棄済）

私は、私自身の知識に基いて本宣言書中で私が行う表明が真実であり、かつ私の入手した情報と私の信じるところに基く表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第 18 編第 1001 条に基き、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行えば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状：私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁護士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number).

Edward D. Manzo (Reg. No. 28, 139)

ここに署名する者は、この申請に関して米国特許商標局においてなされるべき如何なる行動に関しても、ここに指名された米国弁護士または代理人が、米国弁護士または代理人とここに署名した者との間で直接の連絡を取ることなしに、__________________からの指示を受け入れてそれに従う権限を与える。指示を出す人物に変更がある場合は、ここに指名された米国弁護士または代理人は、ここに署名した者からその旨通知を受ける。

The undersigned hereby authorizes any U. S. attorney or agent named herein to accept and follow instructions from __________________ as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U. S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U. S. attorneys or agents named herein will be so notified by the undersigned.

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国籍		Citizenship Japanese
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第三共同発明者名		Full name of third joint inventor, if any
第三共同発明者の署名	日付	Third inventor's signature Date
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国籍		Citizenship
私書箱		Post Office Address

第四共同発明者名		Full name of fourth joint inventor, if any
第四共同発明者の署名	日付	Fourth inventor's signature Date
住所		Residence
国籍		Citizenship
私書箱		Post Office Address